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Abstract A kind of process for fabricating CMOS transistor of IC devices employing double spacers with the capability of preventing short-channel effect is disclosed in the present invention. At first, a gate structure is formed on the substrate of integrated circuit device, and is followed by forming the first isolation layer on the sidewall of the gate structure. After that, impurities are implanted into the source/drain regions of the transistor to form lightly doped source/drain regions of the transistor. Then, the second sidewall isolation layer is formed for the gate structure such that the second sidewall isolation layer covers the surface of the first sidewall isolation layer. By using a source/drain implantation procedure, heavily doped source/drain regions are formed below the lightly doped source/drain regions. At last, by performing a rapid thermal annealing procedure, the impurities of lightly doped source/drain regions and heavily doped source/drain regions are driven in a side direction into the channel region of the transistor. The degree of driving impurities in a side direction into the channel region is substantially equal to the thickness of the first isolation layer at the base of gate structure. In addition, the source/drain regions of the transistor are activated through the rapid thermal annealing procedure.

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